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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,479	11/06/2003	Stephen K. Sunter	LVPAT062US	8598

26668 7590 08/10/2006

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EXAMINER	
NGUYEN, STEVE N	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,479	SUNTER ET AL.	
	Examiner	Art Unit	
	Steve Nguyen	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *8-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Apr. 9, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are currently pending.

Election/Restrictions

2. Claims 8-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 5/31/2006.

Applicant's election with traverse of Invention Group I in the reply filed on 5/31/2006 is acknowledged. The traversal is on the ground(s) that the restriction is improper. This is not found persuasive for the following reasons. Inventions Group I and Group II are related as combination and subcombination, Invention Group I being the subcombination. As detailed in the prior restriction requirement, Invention Group II does not require the particulars of Invention Group I. For example, a conventional tristate buffer can be used in Invention Group II instead of the circuit described by Invention Group I to place the tristate pin drivers in a high-impedance state and de-assert the signal to return to the driving state. A conventional tristate buffer is a materially different apparatus than the circuit of Group I. Invention Group I does not have to be used for testing the function of a pin enable bit of unconnected pins as required in Group II. Invention Group I can be used in the prior art structure of Fig. 3

detailed by the Applicant on page 2 of the specification. The fact that Group I is an apparatus and Groups II and III are directed to a method or process has no bearing on determining the relationship of a combination or subcombination because an apparatus (subcombination) could be used in a method (combination). Inventions Group II and Group III are independent for the reasons provided in the prior restriction requirement. The requirement is still deemed proper and is therefore made FINAL.

Allowable Subject Matter

3. Claims 6 and 7 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Objections

4. Claims 1 and 4 objected to because of the following informalities:

Claim 1 is not properly indented in such a way to delineate the body of the claims from the preamble. It is assumed that the preamble ends with the word "comprising".

The first limitation should be corrected to read, "a tristate control circuit for selectively controlling a pin driver enable input of said pin drivers." Appropriate correction is required.

Claim 4 recites, "first means for combining a TAP Capture-DR state signal and a control input". If Applicant intended "a control input" to be the same "control input" mentioned in claim 1 ("responsive to a control input for temporarily de-asserting a

signal...", Applicant is advised to refer to the control input in claim 4 as "said control input" for clarification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 rejected under 35 U.S.C. 102(b) as being anticipated by Admitted Prior Art (hereinafter referred to as Admission).

As per claim 1:

Admission discloses a boundary scan interface circuit for use with a test access port (TAP) controller for testing the state of pin drivers of an IEEE 1149.1-compliant integrated circuit (IC) having a boundary scan register (Fig. 3), said interface circuit comprising: a tristate control circuit for selectively controlling pin driver enable input of said pin drivers (Fig. 3, element 19; page 2, lines 1-2) and responsive to a control input for temporarily de-asserting a signal that tri-states the pin drivers during a capture cycle of said TAP in which pin logic values are captured by the BSR (Fig. 3, element 23; page 2, lines 6-11).

6. Claim 1 rejected under 35 U.S.C. 102(b) as being anticipated by Levitt (US Pat. 5,513,186).

As per claim 1:

Levitt discloses a boundary scan interface circuit for use with a test access port (TAP) controller (Fig. 2, element 240) for testing the state of pin drivers of an IEEE 1149.1-compliant integrated circuit (IC) having a boundary scan register (Fig. 2, element 222), said interface circuit comprising: a tristate control circuit for selectively controlling pin driver enable input of said pin drivers (Fig. 2, element 270) and responsive to a control input for temporarily de-asserting a signal that tri-states the pin drivers during a capture cycle of said TAP in which pin logic values are captured by the BSR (col. 2, lines 51-52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 2 and 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Admission in view of Nadeau-Dostie et al (US Pat. 6,000,051; hereinafter referred to as Nadeau-Dostie). Note: with respect to claim 3, IEEE 1149.1 is brought in as a teaching reference to further point out features of IEEE 1149.1 employed by both Admission and Nadeau-Dostie.

As per claim 2:

Admission teaches the interface circuit as defined in claim 1 above. Not explicitly disclosed by Admission is the circuit further including: an update control circuit responsive to a second control input for generating a boundary scan cell update signal to provide a first test mode for loading test data into a boundary scan register without updating outputs of said register.

However, Nadeau-Dostie in an analogous art teaches a method for testing high speed interconnectivity of circuit boards in which an update control circuit (Fig. 1, element 26) responsive to a second control input (col. 4, lines 35-38) for generating a boundary scan cell update signal to provide a first test mode for loading test data into a boundary scan register (col. 9, lines 45-52) without updating outputs of said register (col. 9, lines 53-55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the system of Nadeau-Dostie with that of Admission. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have

recognized that the system of Nadeau-Dostie would have provided the additional advantage of testing high speed interconnectivity of circuit boards (col. 2, lines 48-52).

As per claim 3:

IEEE 1149.1 teaches an interface circuit as defined in claim 2, said IC having first and second storage registers for storing first and second control bits (Figs. 8-1 and 8-3 show at least two optional test data registers for storing control bits).

8. Claims 4 and 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Admission in view of Jacobson (US Pat. 6,499,124).

As per claim 4:

Admission teaches an interface circuit as defined in claim 1 above. Not explicitly disclosed by Admission is said tristate control circuit including: first means for combining a TAP Capture-DR state signal and a control input and producing a tristate disabling control signal; and second means for combining a tristating signal and said tristate disabling control signal for producing a pin driver enable control signal.

However, Jacobson in an analogous art teaches a security control circuit (Fig. 7) for combining a TAP Intest signal (Fig. 7, element 724; col. 10, lines 12-14) and a control input (Fig. 7, element 660; col. 8, lines 42-48) and producing a control signal (Fig. 7, element 726; col. 10, lines 14-16); and second means (Fig. 7, element 730) for combining a data signal (Fig. 7, element 672) and the control signal for producing an enable control signal (Fig. 7, element 674).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the security circuit 650 of Jacobson to generate the forceDisable signal of Admission by supplying the input 724 with a Capture-DR signal and input 672 with a tristate disabling signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have been motivated to do so in order to thwart a would-be pirate from replicating the logic captured in the boundary scan register (col. 10, lines 35-38).

As per claim 5:

Jacobson further teaches an interface circuit as defined in claim 4, said tristate disabling control signal being a pulse having a duration of one clock period of a test clock (the pulse must be one period because the memory and TAP components are clocked with a test clock).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steve Nguyen whose telephone number is (571) 272-7214. The examiner can normally be reached on M-F, 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steve Nguyen
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER